One-Dimensional Semiconductor Nanostructure Based Thin-Film Partial Composite Formed by Transfer Implantation for High-Performance Flexible and Printable Electronics at Low Temperature

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ABSTRACT Having high bending stability and effective gate coupling, the one-dimensional semiconductor nanostructures (ODSNs)-based thin-film partial composite was demonstrated, and its feasibility was confirmed through fabricating the Si NW thin-film partial composite on the poly(4-vinylphenol) (PVP) layer, obtaining uniform and high-performance flexible field-effect transistors (FETs). With the thin-film partial composite optimized by controlling the key steps consisting of the two-dimensional random dispersion on the hydrophilic substrate of ODSNs and the pressure-induced transfer implantation of them into the uncured thin dielectric polymer layer, the multinanowire (NW) FET devices were simply fabricated. As the NW density increases, the on-current of NW FETs increases linearly, implying that uniform NW distribution can be obtained with random directions over the entire region of the substrate despite the simplicity of the drop-casting method. The implantation of NWs by mechanical transfer printing onto the PVP layer enhanced the gate coupling and bending stability. As a result, the enhancements of the field-effect mobility and subthreshold swing and the stable device operation up to a 2.5 mm radius bending situation were achieved without an additional top passivation.

KEYWORDS: nanowire · transferring · flexible electronics · partial composite

One-dimensional semiconductor nanostructures (ODSNs), such as nanowires (NWs), nanotubes, and nanoribbons, have significantly exhibited interesting devices with unique properties and advanced potential for various applications that are used in nanoelectronic and nanophotonic devices.[1−5] During the past decade, field-effect transistors (FETs),[6−9] sensors,[10,11] diodes,[12,13] and logic circuits[14,15] based upon ODSNs have been introduced along with the synthesizing strategies for the mass production of them. The technologies for the syntheses of ODSNs have already been developed; on the other hand, the technologies for fabrication of the devices for their electronic applications have not yet been developed. The next 10 years will be important in the development of easy and efficient fabrication routes for these unique nanomaterials.

In the fabrication of devices using ODSNs, a significant issue based upon the conventional photolithographic technique is how to easily and efficiently make thin-film-like monolayers composed of ODSNs, which reside discretely and randomly with each other in a dispersion solution. To overcome this problem, many ideas for the thin-film-like array have been reported, such as electric field directed assembly,[16] flow-assisted alignment,[17] selective chemical patterning,[18] Langmuir−Blodgett,[19] and the blown bubble films technique.[20] The monolayers formed by using the above array strategies show an electrically anisotropic property that is not proper for the thin-film-based device fabrication because these anisotropies require an alignment process step during electrode addressing. Additionally, to preserve performance and prevent form degradation, the passivation has to be conducted after device fabrication based on ODSNs, the surface of which is very vulnerable to contaminants from ambients, such as water molecules, carbon radicals, microdust, and so on. The passivation of these devices with inert material enhances their stability in a bending situation and in gate coupling to the device.

In this study, to satisfy the above-mentioned requirements of an electrically

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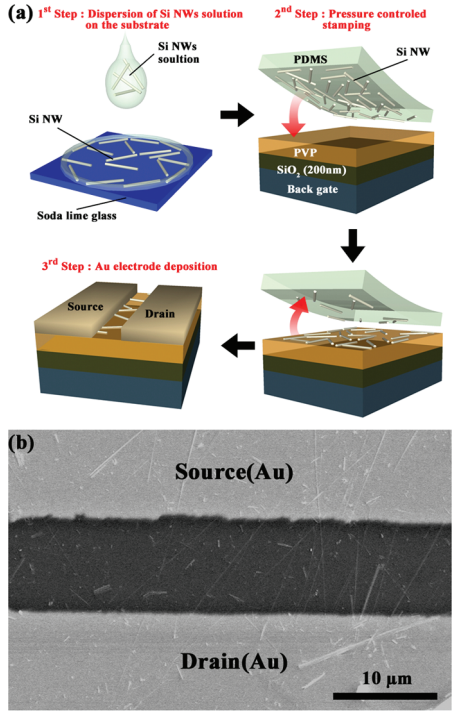

Figure 1. (a) The fabrication process sequence by using the stamping method with a controlled pressure. The well-purified Si NW solution was dispensed on the soda lime glass substrate to get a uniform and random directional Si NW monolayer. The dispersed NWs were moved to the PDMS mold, and the NWs on PDMS were then transferred after cross-linking PVP and before cross-linking PVP for non-implanted and implanted NW FETs, respectively. When transferred from substrate to substrate, dense NWs on the PDMS leave one layer on the coated PVP. Here, the PVP/Si NW composite film performs as a two-dimensional channel. (b) An SEM image of the source and drain electrodes defined by a tungsten wire stencil with a diameter of 8 μm.

isotropic active layer, high bending stability, and effective gate coupling, the ODSN-based thin-film partial composite was introduced. The key steps in the process of forming the thin-film partial composite consist of the two-dimensional random dispersion on the hydrophilic substrate of ODSNs and the pressure-induced transfer implantation of them into the uncured thin dielectric polymer layer. Here, we show the feasibility of our strategy through fabricating the Si NW thin-film partial composite on the poly(4-vinylphenol) (PVP) layer, obtaining uniform and high-performance flexible field-effect transistors (FETs).

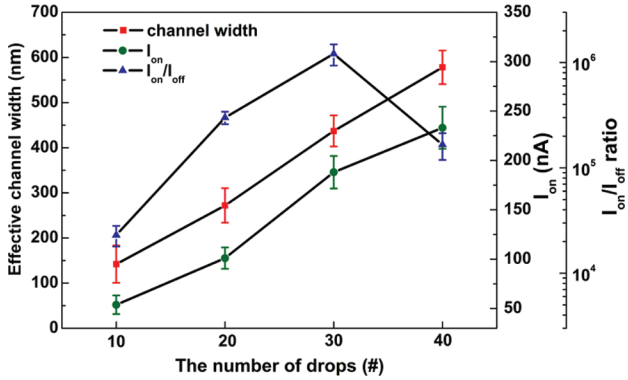

Figure 2. Effective channel width, I_{on}, and I_{on}/I_{off} ratio with varying the number of drops of the NW solution; 10, 20, 30, and 40.

RESULTS AND DISCUSSION

Figure 1a shows the schematic diagrams illustrating the process to fabricate the Si NW thin-film partial composite and FETs. The first step is to dispense tens of drops from a well-purified solution of Si NWs on the soda lime glass substrate to get a uniform and random directional Si NW monolayer. The Si NWs used here are synthesized by an electroless etching process, and the length of the NWs is about 100 μm (see the Supporting Information, Figure S1). The second step is to form a thin-film partial composite, as shown in Figure 1a. The monolayer on the glass substrate is implanted into the uncured PVP layer on the gate electrode by using pressure-controlled stamping through the transferring medium, poly(dimethylsiloxane) (PDMS).[21−23] In this step, the function of the PVP layer is the matrix of the partial composite and gate dielectric. Finally, the source and drain electrodes for the FET were deposited by using thermal evaporation of Au with a tungsten 8 μm wire stencil mask (Figure 1b). The wire stencil mask makes it possible to define the source and drain electrodes without a photolithography process.

When a drop of the Si NW solution is dispensed on the surface of the hydrophilic glass substrate, it spreads out through the entire area, leaving Si NWs at every site where the solution flows over. The density of Si NWs in the random directional monolayer depends on the number of drops and the Si NW solution density. To verify the uniformity of the random Si NW monolayer and reproducibility of this process, the number of drops was varied from 10 to 40, the 64 Si NW FETs for each dropping condition were fabricated, and their effective channel width, on-current (I_{on}), and on/off current ratio were evaluated, as shown in Figure 2. The effective channel width is estimated as the summation of the NW's diameters in the channel area. With the increased number of drops, the effective channel widths increase and the I_{on}'s of the FETs also increase linearly. However, in the case of 40 times dropping, the on/off ratios of the devices decrease due to the NW's aggregation in the high-density composite film. The linearity between the number of drops and the effective channel width implies that a uniform Si NW monolayer can be achieved by using the dropping method on the hydrophilic substrate. As shown in the Supporting Information, Figure S2, it is observed that the directions of the Si NWs were randomly distributed between the source and the direction of the drain electrodes gap.

The depth of the implantation of Si NWs can be modulated by controlling the amount of pressure during transfer of the NWs from the glass to the PVP layer, as shown in Figure 3a−d, where the cross-sectional

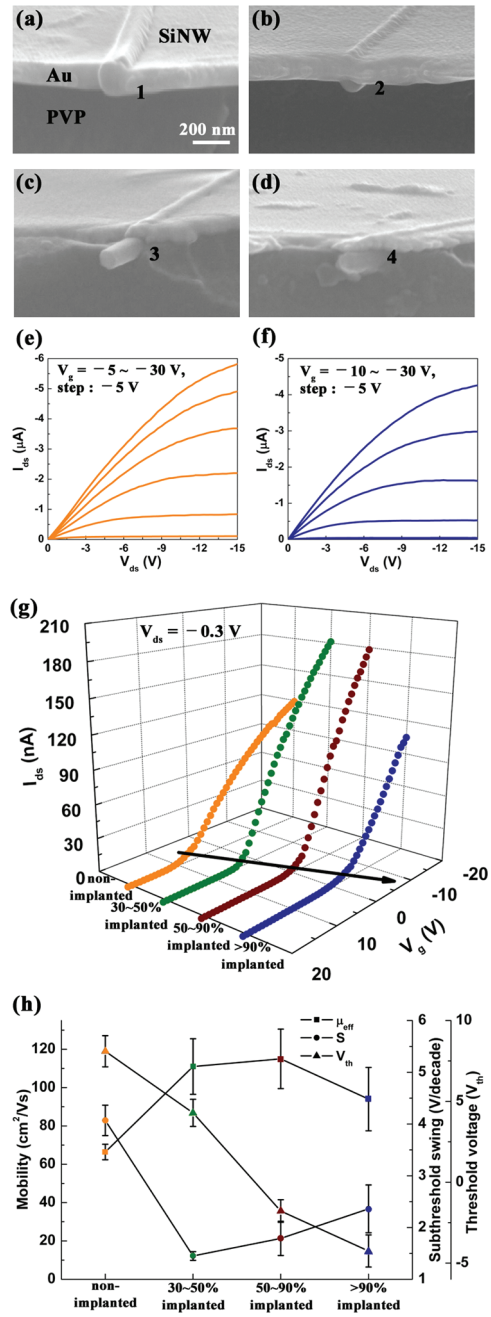

Figure 3. (a−d) SEM images of the nonimplanted state and implanted states of Si NWs on PVP. The three kinds of implanted NW states were prepared by pressing with the controlled pressures of 0, 50, and 200 kPa, respectively. Finally, the implanted states of Si NWs on the PVP dielectric layer were classified as four major types: (a) nonimplanted, (b) implanted below 50%, (c) implanted between 50% and 90%, and (d) implanted above 90%. (e, f) The output characteristics ($I_{ds}-V_{ds}$) of (e) nonimplanted NW FETs and (f) implanted NW FETs. (g) The transfer characteristics ($I_{ds}-V_g$) for each state at a drain voltage of −0.3 V (1−4). The threshold voltage is dramatically changed along the black arrowhead by increasing the implanted degree. (h) The μ_{eff}, S, and V_{th} for the different implanted states.

features represent the states of implantation. The implanted states of the Si NWs on the PVP dielectric layer were classified as four major levels: nonimplanted (1, Figure 3a), implanted below 50% (2, Figure 3b), implanted between 50% and 90% (3, Figure 3c), and implanted above 90% (4, Figure 3d). The device performances were estimated by considering the effective channel width (350−450 nm, 30 drops). The output ($I_{ds}-V_{ds}$) curves at each state were taken at different V_g values ranging from −5 to −30 V in steps of −5 V (Figure 3e,f; see the Supporting Information, Figure S3). The I_{ds} increases with increasing negative V_g and saturates with increasing V_{ds}. These curves show typical p-channel transistor behavior and good Ohmic contact in all sample states. The transfer ($I_{ds}-V_g$) characteristics of the same device at a fixed V_{ds} of −0.3 V are shown in Figure 3g. As the degree of the implantation of Si NWs into the PVP gate dielectric increases, the threshold voltage in the nonimplanted state of the depletion mode in which current flows at a positive voltage was dramatically changed into the enhancement mode in which the current flows at a negative voltage. To quantitatively compare the device performance for different implanted states, the threshold voltage (V_{th}), field-effect mobility (μ_{eff}), and subthreshold swing (S) were determined; the results are exhibited in Figure 3h. The μ_{eff} can be estimated using the following equation, $\mu_{eff} = L/(W \times C_i \times V_{ds}) \times g_m$, from the channel length (L), channel width (W), capacitance per unit area of gate dielectric (C_i), and transconductance (g_m).[24] Because the NWs are not perpendicular to the S/D contact edges, the real L is larger than that of the S/D gap. From the above equation, the μ_{eff} is proportional to the value of L. Therefore, to avoid the ambiguous evaluation of μ_{eff}, we choose the length of the S/D gap as a minimum L for the calculation of the μ_{eff}. The devices with the implanted states exhibited a higher μ_{eff} and I_{on}/I_{off} ratio than those with nonimplanted states. The S values of the implanted cases were also superior to those of the nonimplanted ones. The details of the electrical properties of each case are summarized in Table S4 in the Supporting Information.

The electrical properties of p-type Si NWs, synthesized by the electroless etching method, were generally operated by the depletion mode.[25,26] One can understand the transition behavior of the operating mode by considering the surface condition of Si NWs. In the primary state, the rough Si NWs have a high density of surface states, and thus, they can be expected to retain much more adsorbed sites on the surface than the smooth NWs. The absorbed negative charges (OH^- ion) on the rough surfaces of Si NWs would cause the surface band bending and lead to accumulation of excess holes in the valence band, resulting in the depletion mode.[25,27] In contrast, when the Si NWs are implanted into the PVP layer by simple pressing, these OH^- ions are reduced with the curing PVP that wraps around the NW surface. This situation brings about the decrease in excess carrier concentration in the conduction channel, and subsequently, a considerable shift of V_{th} toward zero voltage appears in the TFT perfor-

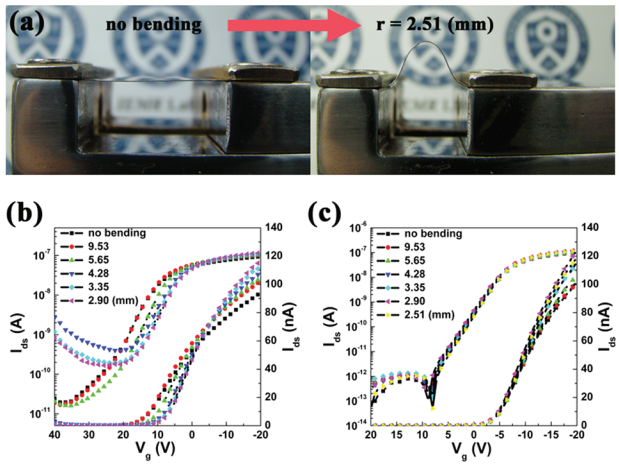

Figure 4. (a) Photograph of flexible devices in the bending machine. Two states, no bending and bending up to 2.51 mm, are shown. The transfer characteristics of the devices with varying the bending radius: (b) nonimplanted and (c) implanted above 90%.

mance. Moreover, for the more deeply implanted devices, the significant shifts in threshold voltages can be attributed to the increased scattering effect. The carrier trapping on the surface between NWs and the PVP polymer increasingly causes delay of the turn-on gate voltage.[28]

As shown in Figure 3h, compared with the nonimplanted Si NW FETs, the implanted Si NW FETs show relatively high I_{on} and μ_{eff} because the effective channel area, coupled by gate bias increases and defect states by the surface passivation, decreases as the NWs get deeper into PVP. Especially in defect states caused by OH^- ions, the NW appears as a large shift of the hysteresis loop.[29] These hysteresis loop shifts become smaller as the NW is gradually implanted (Supporting Information, Figure S5) because the defect states are passivated by the PVP dielectric layer. In addition, the subthreshold slopes are enhanced as the implantation depth increases. The enhancement of the subthreshold slope may be due to the decrease of defect states by passivation,[30] although implantation above 90% (4, Figure 3d) deteriorates because of poor contact between Si NWs and Au.

To analyze gate couplings for various implanted conditions of Si NWs, the cross-sectional charge distributions around channel regions were simulated by using Silvaco's ATLAS, a two-dimensional electronic device simulator. In this case, the characteristics of $C-V$ were simulated by fitting the values of the parameter of the discrete interface trap state related to the $C-V$ slope with the values of the parameter of the interface trap charge related to the total capacitance and flat band. Interfacial characteristic parameters between the NW and the PVP dielectric layer were assumed from the previous calculation and applied to simulation of effective distance effects on $C-V$ characteristics as the degree of implantation increases. The results of the $C-V$ plot for that are exhibited in the Supporting Information, Figure S6. Figure S6a in the Supporting Information shows a $C-V$ characteristic of the PVP gate dielectric by degree of implanted depth from simulations and the electric field in which NWs were received was calculated. The thickness of the PVP dielectric and the radius of the NW were defined as 480 and 50 nm, respectively. It is clearly seen that the deeper implanted state leads to a distance reduction between the gate electrode and the center of the NW, which results in higher carrier density around the NW due to the increased capacitance and also an enlarged effective conducting channel area on the surface of the NW. Considering the SiO_2 dielectric (200 nm, $C_{ox} = 16.9$ nF/cm^2) of the series structure, the total capacitances per unit area of the gate dielectric (C_i) were calculated to be 6.13, 6.22, 6.32, and 6.44 nF/cm^2 as grades of implanted depth. As expected, a nonuniform potential distribution formed on the surface when the NW was not implanted into the PVP. In this case, the minimum potential occurs at a point off the center of the NW away from the gate. The potential reaches a maximum at the edge of the NW that touches the PVP. However, the charge distribution of the implanted NW surface is more homogeneous than that of the nonimplanted one. The net space charge distribution according to the implanted state can be seen in the Supporting Information, Figure S6b−e.

To determine bending stability, we fabricated flexible NW FETs for varying the implantation depth of NWs. Figure 4a shows the flexible device having a bending radius of 2.51 mm. For the nonimplanted device, the μ_{eff}, V_{th}, and I_{on}/I_{off} ratio change by varying the bending radius (Figure 4b). On the other hand, for the device implanted above 90%, the performances were almost unchanged to a high bending radius up to 2.51 mm (Figure 4c). From these results, it is believed that devices made of the implanted NWs show excellent mechanical bending stability because the implanted NWs are more strongly grasped by the cross-linked PVP. For the flexible device implanted above 90%, a bending stability test was carried out (Supporting Information, Figure S7). The mechanical stability of the same device was ensured over 2000 times. Except for the aging effect between 0 and 10 times, no significant change in the electrical properties was observed until 2000 times.

CONCLUSION

In conclusion, a thin-film partial composite based upon ODSNs was introduced to achieve an electrically isotropic active layer, high bending stability, and effective gate coupling for FETs. A simple drop-casting of NW solution and a pressure-induced transferring implantation controlled the number of drops and the amount of pressure. The partial composite films were fabricated with varying NW densities and the depths of implantation. As the NW density increases, the I_{on} of NW FETs in-

creases linearly, implying that a uniform NW distribution can be obtained with random directions over the entire region of the substrate despite the simplicity of the drop-casting method. In particular, in our fabrication process, it was found that the implantation of NWs by mechanical transfer printing onto the PVP layer enhanced the gate coupling and bending stability of the NW FETs because the NWs were surrounded by the stable polymer, dielectric, and insulator materials. Actually, superior μ_{eff} and S were achieved in the implanted cases, and up to a 2.5 mm radius bending situation, the implanted NW FETs exhibited stable operating characteristics without an additional top passivation. We believe that the ODSN thin-film partial composite formed by transfer implantation will be a component in the highly flexible and printable electronics at low temperatures in various nanomaterial-based electronics and optoelectronics applications.

EXPERIMENTAL METHODS

Synthesis of Si NWs. A boron-doped p-type Si(100) wafer with a resistivity of 1−10 Ω · cm was used as a starting wafer for the synthesis of Si NWs. The wafers were rinsed with trichloroethylene, acetone, ethanol, and deionized (DI) water. To remove the silicon dioxide on the silicon surface, the RCA cleaning was performed before the NW synthesis steps. Ag nanoparticles, which act as a catalyst of electroless etching, were coated on the Si substrate with an electroless metal deposition (EMD) by dipping in the mixture solution of 10% HF and 0.02 M $AgNO_3$ for 1 min at room temperature. The residual Ag dendrite formed during the EMD process was removed with DI water, and then the Si substrate was immersed in an etching solution of 10% HF and 0.6% H_2O_2 for 2 h at 50 °C. After the electroless etching process, the substrate having Si NWs was washed by using 5% HF and DI water, respectively, to remove residual oxide and extra remnants. The synthesized Si NWs were structurally analyzed using field emission scanning electron microscopy (FESEM, JEOL JSM-6500F) and high-resolution transmission electron microscopy (HRTEM, JEOL JSM-2100F) (Supporting Information, Figure S1).

Fabrication and Characterization of Si NW FETs. The synthesized Si NWs were detached from the Si wafer by a blade and then dispersed in isopropyl alcohol (IPA) by using sonication. To collect Si NWs with a diameter below 120 nm, the centrifugation machine was used at 5000 rpm. The rectified NWs solution was spread several times on a slide glass substrate until the intended density was achieved. The dispersed NWs on the substrate were transferred on poly(dimethylsiloxane) (PDMS) by contact, and then NWs on PDMS were stamped on the poly(4-vinylphenol) (PVP) dielectric layer as an adhesive layer with varied press pressures. The PVP film was prepared by a 10 wt % PVP solution, which was composed of a cross-linker, poly(melamine-*co*-formaldehyde), and a solvent, propylene glycol monomethyl ether acetate (PGMEA). The solution was coated on degenerately doped p-type Si substrates with 200 nm thick SiO_2 gate dielectrics by using a spin-coater. For cross-linking of coated PVP, the latter was cured for 60 min at 175 °C using an oven. The fabricated Si NW FET devices were categorized into four major types: nonimplanted and three kinds of implanted NW FET device structures. The dispersed NWs on PDMS were transferred on after cross-linking PVP and before cross-linking PVP, respectively, in case of nonimplanted and implanted NW FETs. The three kinds of implanted NW FETs (Figure 3b−d) were fabricated by pressing with the controlled pressures of 0, 50, and 200 kPa, respectively. The source and drain electrodes, which were deposited by a thermal evaporation of Au, were defined by a tungsten wire stencil with a diameter of 8 μm in a structure of Si NW FETs. The current−voltage ($I-V$) measurements of the Si NW FETs were carried out using a semiconductor parameter analyzer (HP 4145B).

Fabrication and Characterization of Si NW Flexible FETs. To fabricate the Si NW flexible device, the polyimide (PI) substrate was cut into a 2 × 2 cm fragment and deposited by the Al gate. The gate dielectric layer was coated by a solution of 10 wt % PVP by using a spin-coater and then cured. For the second PVP, an adhesive as well as a dielectric layer was prepared, and implanted and nonimplanted flexible devices were fabricated by the above method. The substrate was put on the bending machine with a 20 mm gap, and $I-V$ characteristics were measured in gap decrements of 1 mm.

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Supporting Information Available: The contents of the Supporting Information include the following: (1) SEM and TEM images of a synthesized Si NW, (2) SEM images of NW distribution with varying the number of drops, (3) output characteristics ($I_{ds}-V_{ds}$) of each implanted states, (4) the electrical properties in each state, (5) the transfer characteristics for the different implanted states, (6) the $C-V$ characteristics and electric field contour on Si NWs from the PVP layer, and (7) the bending stability test results for the flexible device implanted above 90%. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Duan, X.; Huang, Y.; Cui, Y.; Wang, J.; Lieber, C. M. Indium Phosphide Nanowires as Building Blocks for Nanoscale Electronic and Optoelectronic Devices. *Nature* **2001**, *409*, 66–69.
2. Huang, M. H.; Mao, S.; Feick, H.; Yan, H.; Wu, Y.; Kind, H.; Weber, E.; Russo, R.; Yang, P. Room-Temperature Ultraviolet Nanowire Nanolasers. *Science* **2001**, *292*, 1897–1899.
3. Goldberger, J.; He, R.; Zhang, Y.; Lee, S.; Yan, H.; Choi, H. J.; Yang, P. Single-Crystal Gallium Nitride Nanotubes. *Nature* **2003**, *422*, 599–602.
4. Duan, X.; Niu, C.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. L. High-Performance Thin-Film Transistors Using Semiconductor Nanowires and Nanoribbons. *Nature* **2003**, *425*, 274–278.
5. Wang, Z. L.; Song, J. Piezoelectric Nanogenerators Based on Zinc Oxide Nanowire Arrays. *Science* **2006**, *312*, 242–246.
6. Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. High Performance Silicon Nanowire Field Effect Transistors. *Nano Lett.* **2003**, *3*, 149–152.
7. Greytak, A. B.; Lauhon, L. J.; Gudiksen, M. S.; Lieber, C. M. Growth and Transport Properties of Complementary Germanium Nanowire Field-Effect Transistors. *Appl. Phys. Lett.* **2004**, *84*, 4176–4178.
8. Moon, K. J.; Choi, J. H.; Lee, T. I.; Ham, M. H.; Maeng, W. J.; Hwang, I.; Kim, H.; Myoung, J. M. Electrical Transport Properties in Electroless-Etched Si Nanowire Field-Effect Transistors. *Microelectron. Eng.* **2010**, *87*, 2407–2410.
9. Choi, J. H.; Lee, S. W.; Kar, J. P.; Das, S. N.; Jeon, J. H.; Moon, K. J.; Lee, T. I.; Jeong, U. Y.; Myoung, J. M. Random Network Transistor Arrays of Embedded ZnO Nanorods in Ion-Gel Gate Dielectric. *J. Mater. Chem.* **2010**, DOI: 10.1039/c0jm01313g.

10. Cui, Y.; Wei, Q.; Park, H.; Lieber, C. M. Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species. *Science* **2001**, *293*, 1289–1292.
11. Lee, J. W.; Moon, K. J.; Ham, M. H.; Myoung, J. M. Dielectrophoretic Assembly of GaN Nanowires for UV Sensor Applications. *Solid State Commun.* **2008**, *148*, 194–198.
12. Qian, F.; Gradečak, S.; Li, Y.; Wen, C. Y.; Lieber, C. M. Core/Multishell Nanowire Heterostructures as Multicolor, High-Efficiency Light-Emitting Diodes. *Nano Lett.* **2005**, *5*, 2287–2291.
13. Jeong, M. C.; Oh, B. Y.; Ham, M. H.; Lee, S. W.; Myoung, J. M. ZnO-Nanowire-Inserted GaN/ZnO Heterojunction Light-Emitting Diodes. *Small* **2007**, *3*, 568–572.
14. Kovtyukhova, N. I.; Mallouk, T. E. Nanowires as Building Blocks for Self-Assembling Logic and Memory Circuits. *Chem.—Eur. J.* **2002**, *8*, 4354–4363.
15. Jo, G.; Hong, W. K.; Maeng, J.; Choe, M.; Park, W.; Lee, T. Logic Inverters Composed of Controlled Depletion-Mode and Enhancement-Mode ZnO Nanowire Transistors. *Appl. Phys. Lett.* **2009**, *94*, 173118.
16. Smith, P. A.; Nordquist, C. D.; Jackson, T. N.; Mayer, T. S.; Martin, B. R.; Mbindyo, J.; Mallouk, T. E. Electric-Field Assisted Assembly and Alignment of Metallic Nanowires. *Appl. Phys. Lett.* **2000**, *77*, 1399–1401.
17. Huang, Y.; Duan, X.; Wei, Q.; Lieber, C. M. Directed Assembly of One-Dimensional Nanostructures into Functional Networks. *Science* **2001**, *291*, 630–633.
18. Auvray, S.; Derycke, V.; Goffman, M.; Filoramo, A.; Jost, O.; Bourgoin, J. P. Chemical Optimization of Self-Assembled Carbon Nanotube Transistors. *Nano Lett.* **2005**, *5*, 451–455.
19. Jin, S.; Whang, D.; McAlpine, M. C.; Friedman, R. S.; Wu, Y.; Lieber, C. M. Scalable Interconnection and Integration of Nanowire Devices without Registration. *Nano Lett.* **2004**, *4*, 915–919.
20. Yu, G.; Cao, A.; Lieber, C. M. Large-Area Blown Bubble Films of Aligned Nanowires and Carbon Nanotubes. *Nat. Nanotechnol.* **2007**, *2*, 372–377.
21. Kang, S. J.; Park, Y. J.; Hwang, J.; Jeong, H. J.; Lee, J. S.; Kim, K. J.; Kim, H. C.; Huh, J.; Park, C. Localized Pressure-Induced Ferroelectric Pattern Arrays of Semicrystalline Poly(vinylidene fluoride) by Microimprinting. *Adv. Mater.* **2007**, *19*, 581–586.
22. Choi, J. H.; Kar, J. P.; Khang, D. Y.; Myoung, J. M. Enhanced Performance of ZnO Nanocomposite Transistor by Simple Mechanical Compression. *J. Phys. Chem. C* **2009**, *113*, 5010–5013.
23. Lee, T. I.; Choi, W. J.; Moon, K. J.; Choi, J. H.; Kar, J. P.; Das, S. N.; Kim, Y. S.; Baik, H. K.; Myoung, J. M. Programmable Direct-Printing Nanowire Electronic Components. *Nano Lett.* **2010**, *10*, 1016–1021.
24. Unalan, H. E.; Yang, Y.; Zhang, Y.; Hiralal, P.; Kuo, D.; Dalal, S.; Butler, T.; Cha, S. N.; Jang, J. E.; Chremmou, K.; Lentaris, G.; Wei, D.; Rosentsveig, R.; Suzuki, K.; Matsumoto, H.; Minagawa, M.; Hayashi, Y.; Chhowalla, M.; Tanioka, A.; Milne, W. I.; Tenne, R.; Amaratunga, G. A. J. ZnO Nanowire and WS_2 Nanotube Electronics. *IEEE Trans. Electron Devices* **2008**, *55*, 2988–3000.
25. Jie, J.; Zhang, W.; Peng, K.; Yuan, G.; Lee, C. S.; Lee, S. T. Surface-Dominated Transport Properties of Silicon Nanowires. *Adv. Funct. Mater.* **2008**, *18*, 3251–3257.
26. Zhang, M. L.; Peng, K. Q.; Fan, X.; Jie, J. S.; Zhang, R. Q.; Lee, S. T.; Wong, N. B. Preparation of Large-Area Uniform Silicon Nanowires Arrays through Metal-Assisted Chemical Etching. *J. Phys. Chem. C* **2008**, *112*, 4444–4450.
27. Kirhara, K.; Kawaguchi, K.; Shimizu, Y.; Sasaki, T.; Koshizaki, N.; Soga, K.; Kimura, K. Dependence of Photocurrent in Single-Crystalline Boron Nanobelts on Atmosphere. *Appl. Phys. Lett.* **2006**, *89*, 243121.
28. Street, R. A.; Salleo, A.; Chabinyc, M. L. Bipolaron Mechanism for Bias-Stress Effects in Polymer Transistors. *Phys. Rev. B* **2003**, *68*, 085316.
29. Lee, E. G.; Wouters, D. J.; Willems, G.; Maes, H. E. Voltage Shift and Deformation in the Hysteresis Loop of Pb(Zr, Ti)O_3 Thin Film by Defects. *Appl. Phys. Lett.* **1996**, *69*, 1223–1225.
30. Klauk, H.; Halik, M.; Zschieschang, U.; Schmid, G.; Radlik, W.; Weber, W. High-Mobility Polymer Gate Dielectric Pentacene Thin Film Transistors. *J. Appl. Phys.* **2002**, *92*, 5259–5263.